VAX-MASSBUS SC750/SC780

INSTALLATION DIAGNOSTIC SOFTWARE (IMD000)

USER'S GUIDE

3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

VX9950912 Rev C
February 1986

Printed in U S A.

TABLE OF CONTENTS

BLANK

Section 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual is designed to serve as a quide for those usinq the Emulex VAX-MASSBUS SC750/SC780 Installation Diagnostic. IMD000- on Digital Equipment Corporation (DEC) VAX-11 computers. IMD000 is designed to run under the Emulex VAX Monitor. EVM.

This utility is designed for use by qualified installers of Emulex equipment. and thus it assumes that the user has some knowledge of hardware configurations. VAX architecture and terminoloqy. and interpretation of error messages and device register contents.

The document contains two main sections:

Section 1	General Description: This section contains an overview of the IMD000 installation diagnostic, includinq its functions. hardware and software compatibility. distribution media. and related documentation.
Section 2	Operation: Describes operation of IMD000 includinq load and start procedures, diagnostic tests. and sample output.

1.2 PRODUCT OVERVIEW

IMD000 is a diagnostic module that is designed for installation and verification of Emulex VAX disk controllers. This diagnostic emulates DEC RM03- RM05- and RM80-

Tests are organized in a proqressive manner, such that each test is more likely to run if the previous test ran successfully; however, tests can be run independently. The first six tests verify hardware existence and verify that the address and data path is clear. The remaininq tests verify major functions of the controller. Tests 20 through 26 may require a formatted disk pack in order to prevent unexpected errors.

Because this program is basically an installation and verification diaqnostic, it does not check for the reliability of data transfer between the host and the mass storage device. This function is performed by a reliability diagnostic proqram. Therefore, runninq this diaqnostic does not destroy user data. and a scratch disk pack is not required.

1.3 DISTRIBUTION MEDIA

The following table lists and describes distribution media for IMD000.

Emulex P/N	Description
VX9960406	TU58 cassette for VAX-11/750
VX9960506	Eight-inch floppy diskette for VAX-11/780
VX9960910	9-track mag tape for VAX-8600

1.4 COMPATIBILITY

1.4.1 HARDWARE

IMD000 will run on any DEC VAX-11/750 or 11/780 system with the following minimum hardware:

- Console device
- 256K bytes memory
- SC750 or SC780 disk controller
- SMD-type disk drive (CDC, Fujitsu, Ampex, etc.)

1.4.2 SOFTWARE

IMD000 is designed to run under the Emulex VAX Monitor, EVM. For more detailed information regarding EVM, see the EVM User's Guide, referenced in subsection 1.5 of this document.

1.5 RELATED DOCUMENTATION

Title: Emulex VAX Monitor (EVM) User's Guide
Publication Number: VX9950901
Publisher: Emulex Corporation
3545 Harbor Blvd.
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

Related Documentation

Title:	SC750/B1 SC750/B3 (RM03/RM05/RM80 Compatible) Disk Controller Technical Manual
Publication Number:	SC7551001
Publisher:	Emulex Corporation 3545 Harbor Blvd. Costa Mesa, CA 92626 (714) 662-5600 TWX 910-595-2521

Title:	SC780/B2 (RP04/RP05/RP06 Compatible) Disk Controller Technical Manual
Publication Number:	SC7851002
Publisher:	Emulex Corporation 3545 Harbor Blvd. Costa Mesa, CA 92626 (714) 662-5600 TWX 910-595-2521

BLANK

Section 2
OPERATION

2.1 OVERVIEW

This subsection describes IMD000 load and start procedures, defines the tests available with IMD000, and presents sample output.

2.2 LOAD AND START PROCEDURES

The procedure used to invoke EVM varies from one VAX system to another. For a description of EVM bootstrapping procedures, see the Emulex VAX Monitor (EVM) User's Guide (reference given in subsection 1.5).

2.2.1 LOAD PROCEDURE

After the EVM> prompt has appeared on the screen, type the following:

EVM>**LOAD IMD000<return>**

The LOAD statement is followed by a SET CONFIGURATION statement, the content of which depends upon the configuration of the VAX system being used. Sample configure statements are presented in the following subsections. For information regarding EVM command syntax and abbreviations, see the EVM user's guide.

2.2.2 DEVICE LINK TABLE

IMD000 has the following default hardware configuration defined in the device link table for both the VAX-11/750 and the VAX-11/780:

Transfer request (TR) level	10
Bus request (BR) level	5
Unit under test (DR)	0
Control status register (CSR)	Supplied by EVM
Interrupt vector	154 hex
UNIBUS bus request (UBR) level	5
Adapter number (AD)	2

2.2.3 SAMPLE CONFIGURE AND START STATEMENTS FOR VAX-11/750

The following sample user input (in **bold** type) sets the default adapter to 3, the unit under test to 5, and the bus request level to 6, and starts tests 1 through 26 in three passes:

```
EVM>SET CON/AD:3/DR:5/BR:6<return>
EVM>ST/T:1:26/PASS:3<return>
```

If no range of test numbers is specified. the monitor assumes that all tests are to be run. The number of passes needs to be specified only if more than one pass is desired; the default value is 1

2.2.4 SAMPLE CONFIGURE AND START STATEMENTS FOR VAX-11/780

The following sample user input (in **bold** type) sets the transfer request level to 12. the unit under test to 3. and the bus request level to 6. and starts tests 1 through 26 in three passes:

```
EVM>SET CON/TR:12/DR:3/BR:6<return>
EVM>ST/T:1:26/PASS:3<return>
```

If no range of test numbers is specified. the monitor assumes that all tests are to be run. The number of passes needs to be specified only if more than one pass is desired; the default value is 1.

2 2.5 DEBUGGER

Entering **<ctrl-c>** (pressing the control and C character keys simultaneously) interrupts the current process and enables you to either continue. abort. or enter a debugging session:

```
EVM>CONTINUE<return>
EVM>ABORT<return>
EVM>DEB<return>
```

If the DEBUG command is entered. the prompt DEB> appears on the screen. The following sample dialog illustrates use of the debugger. (Explanatory comments at right will not appear on the screen.)

```
DEB>EX R0:R10                    ! Lets you examine the GPRs
DEB>DEF BASE=2000                ! Defines a symbol BASE whose
                                   address = 2000 (X)
DEB>EX BASE+12                   ! Examine location
                                   (2000+12)(X)
DEB>DEP .=01                     ! Deposits a new value at this
                                   location
DEB>EXIT                         ! Exits the debugger and
                                   prompts EVM
EVM>
```

For additional information regarding the DEBUG command. see the EVM User's Manual.

2.3 TESTS

The 26 diagnostic tests available with IMD000 are described in the following subsections. After IMD000.EXE has been loaded. information regarding a given test section can also be obtained by typing the **HELP (H)** command. The following sample input would generate descriptions of all 26 tests:

```
EVM>HELP/T:1:26<return>
```

See the EVM User's Guide for more information regarding the HELP command.

For information regarding the registers and bits mentioned in the following subsections. see the appropriate disk controller technical manual referenced in subsection 1 5

2 3.1 TEST 1: MBA AND DRIVE REGISTERS VALIDATION TEST

This test reads the map register and MBA and drive registers in order to verify that they exist. Register contents are ignored during the test. and the test fails if a bus timeout occurs for any register transfer.

2 3.2 TEST 2: MBA REGISTER INIT TEST

This test verifies that the MBA and drive registers can be cleared by MBA init. It loads known data into MBACR and MBADR. reads it back. and verifies good data. It also performs an MBA init to clear MBA registers. verifies that MBACR and MBASR are cleared. and sets MBADR to BF(X).

2.3.3 TEST 3: DRIVE REGISTER INIT TEST

This test verifies that all seven drive registers can be cleared by MBA init. It loads known data into RMCS1 and RMDA. reads them back. and verifies good data to ensure that these registers can be written properly. The test performs an MBA init to clear the drive registers. and verifies that RMCS1. RMDA. RMER1. RMER2. and RMAS are cleared. The ERR. ATA. and LST bits in RMDS are reset. and RMMR1 is set to 8(X).

2 3.4 TEST 4: ADDRESS AND DATA PATH TEST

This test uses the special characteristics of the byte count register to verify that the address and data path of the bus is not shorted or open. The test writes several test patterns into MBABCR. reads it back. and verifies that the data pattern does not change between the upper word and lower word of MBABCR.

2.3.5 TEST 5: TEST BITS IN MBA MAP REGISTERS

This test verifies write/read of all 256 map registers. It writes a unique pattern in each map register. reads them back. and verifies good data. The test complements each map register and verifies that the rest of the map registers do not change. It verifies the loading and reading of all read/write bits for each map register with both a floating zeros and a floating ones pattern.

2 3.6 TEST 6: DRIVE CLEAR TEST

This test writes all ones into each of the write/read registers, and then issues a drive clear command. It verifies that all the bits were cleared.

2.3.7 TEST 7: ILLEGAL REGISTER TEST

This test reads all valid drive registers (00(X) - 3C(X)) and verifies that there are no error sets. It reads all invalid drive registers (40(X) - 7C(X)) and checks for "ILR" sets in RMER1; data in the lower 16 bits will be zeros. A drive clear is performed between reads.

2 3.8 TEST 8: MBASR UPPER 16 BIT TEST

This test sets the STMATTN bit in MBADR and verifies that the ATTN bit in MBASR is set. It reads all drive registers and verifies that the upper 16 bits of MBASR reads out as the upper 16 bits of any drive register.

2.3.9 TEST 9: ATA AND ERR BITS TEST

This test verifies that the ATA and ERR bits set and reset properly. It performs the following steps:

1. Write to RMER1. ATA and ERR should be set.
2. Write to RMAS Verify that ERR = 1 and ATA = 0
3. Write zeros to RMER1. ATA should be set and ERR should be reset
4. Write to RMER1 and execute a drive clear. Verify that ATA and ERR are zeros.

2.3.10 TEST 10: TEST ATTENTION INTERRUPT WITH/WITHOUT IE SET

This test includes two subtests: It verifies that asserting ATTN in MBASR causes an interrupt to the CPU if IE is set. and it verifies that asserting ATTN in MBASR does not cause an interrupt to the CPU if IE is not set.

2 3.11 TEST 11: ILLEGAL FUNCTION CODE TEST

This test verifies that ILF (bit 0 of RMER1) is OFF for legal function codes and ON for illegal function codes: 0A. 0B. 0D. 0E. 0F. 10. 11. 12. 13. 16. 17. 1A. 1B. 1E, 1F.

2.3.12 TEST 12: QUALIFICATION TEST

This test verifies the presence of RM03/RM05 or RM80 at the addresses specified by the operator. It verifies that the MASSBUS is alive and that a drive under test exists and is available. The test checks the following bits: NED. DVA. VV. MOL DPR. and DRY.

2.3.13 TEST 13: READ IN PRESET TEST WITH RMOF. RMDA. AND RMDC

This test includes two subtests. The first subtest verifies that the Read In Preset command resets the FMT16. ECI. and HCI bits in the RMOF register. The second subtest verifies that the Read In Preset command resets the desired cylinder address and the disk address. RMDA and RMDC are preset and tested for zero after the Read In Preset command.

2 3.14 TEST 14: OFFSET AND RETURN TO CENTER LINE TEST

This test verifies that an offset command can be executed from and to each offset value. It then verifies that a Return to Center Line command can be executed without error. The test verifies that the OFM bit in the RMDS register can be set and cleared correctly.

2.3.15 TEST 15: SEEK OPERATION TEST

This test performs a seek operation with valid disk address. It starts with cylinder address 1. and then increments the cylinder address by walking through each bit in the address until the maximum address is reached. The test verifies that ATA in RMAS is set properly.

2.3.16 TEST 16: TEST IAE WITH INVALID SECTOR ADDRESS

This test issues a controller clear and sets the invalid sector address by resetting FMT16 in RMOF. It verifies that IAE is set by executing the search command with FMT16 reset.

2.3.17 TEST 17: TEST IAE WITH INVALID TRACK ADDRESS

This test issues a controller clear and performs a seek operation with an invalid track address. It verifies that IAE is set.

2.3.18 TEST 18: TEST IAE WITH INVALID CYLINDER ADDRESS

This test issues a controller clear and performs a seek operation with an invalid cylinder address. It verifies that IAE is set.

2.3.19 TEST 19: INTERRUPT TEST

This test verifies that an interrupt occurs after either a positioning command or completion of a data transfer. It executes a Read Data and a Recalibrate with interrupts enabled, and verifies that an interrupt occurred and that no errors occurred.

2.3.20 TEST 20: RECALIBRATION FUNCTION TEST

This test issues a Recalibrate command to the test drive. It sets up a short timer, then executes a Read Header and Data command with byte count = 4. The test verifies that the Recalibrate command works properly (if a timeout does not occur) and checks the header data.

2.3.21 TEST 21: ADDRESS OVERFLOW ERROR TEST

This test issues a controller clear and performs a two sectors read operation, starting with the last sector of the last cylinder. It verifies that AOE is set in the RMER register and that LST is set in the RMDS register.

2.3.22 TEST 22: LAST SECTOR TRANSFER TEST

This test issues a controller clear and performs a read operation, starting with the last sector and last track of the last cylinder. It verifies that the LST bit is set in the RMDS register.

2.3.23 TEST 23: TEST DMA READ WITH INVALID MAP REGISTERS

This test verifies that a DMA read operation with the map register valid bit (bit 31) not set causes the DTA. DTC. and IM bits in the MBA Status Register to be set.

2.3.24 TEST 24: REGISTER MODIFICATION REFUSED TEST

This test verifies that REGISTER MODIFICATION REFUSED is set when a write is written to any drive register (except RMAS) is attempted with DRY reset and GO set.

2.3.25 TEST 25: DATA TRANSFER ABORT TEST

This test issues a controller clear and performs a four sectors read operation. The test attempts to set ABT in MBACR when DTB is set. and verifies that PGE is not set. DTA is set. and the MBA Byte Count Register is not equal to 0.

2.3.26 TEST 26: READ HEADER AND READ DATA TEST

This test executes the Read Header and Data command and the Read Data command from sector 0. track 0. cylinder 0. with the byte count equal to the maximum sector number. The test progresses from sector 0. track 0. cylinder 0 to the last sector. track. and cylinder address. After each transfer. the status of the controller is checked for any errors that have occurred.

2.4 SAMPLE OUTPUT

The program announces itself and then prints out the title of each test. followed by a summary report. In this example. the operator did not use any command qualifiers with ST (START). so the program will run one pass of all 26 tests. Note that. in some instances. output has been continued to a second line of text here because of space limitations.

```
EVM>ST<return>

EMULEX VAX-MASSBUS SC7000/SC750/SC780 INSTALLATION DIAGNOSTIC
REV 1 0  12-OCT-1984 9:9:28

CPU ID = 00000002. VAX-11/750

DRIVE UNIT: 1
DRIVE CONFIGURATION: RM05 (823 Cylinders. 19 Tracks. 32 Sectors)
```

```
TEST # 1 MBA and Drive Registers Validation Test  12-OCT-1984
9:9:28
TEST # 2 MBA Register Init Test  12-OCT-1984 9:9:29
Test # 3 Drive Register Init Test  12-OCT-1984 9:9:31
Test # 4 Address and Data Path Test  12-OCT-1984 9:9:33
Test # 5 Test Bits In MBA Map Registers  12-OCT-1984 9:9:35
Test # 6 Drive Clear Test  12-OCT-1984 9:9:36
Test # 7 Illegal Register Test  12-OCT-1984 9:9:36
Test # 8 MBASR Upper 16-bit Test  12-OCT-1984 9:9:42
Test # 9 'ATA' and 'ERR' Bits Test  12-OCT-1984 9:9:43
Test # 10 Test Attention Interrupt With/Without 'IE' Set  12-
OCT-1984 9:9:44
Test # 11 Illegal Function Code Test  12-OCT-1984 9:9:46
Test # 12 Oualification Test  12-OCT-1984 9:9:47
Test # 13 Read In Preset Test with RMOF. RMDA and RMDC  12-OCT-
1984 9:9:47
Test # 14 Offset and Return to Center Line Test  12-OCT-1984
9:9:49
Test # 15 Seek Operation Test  12-OCT-1984 9:9:55
Test # 16 Test 'IAE' With Invalid Sector Address  12-OCT-1984
9:10:6
Test # 17 Test 'IAE' With Invalid Track Address  12-OCT-1984
9:10:12
Test # 18 Test 'IAE' With Invalid Cylinder Address  12-OCT-1984
9:10:17
Test # 19 Interrupt Test  12-OCT-1984 9:10:18
Test # 20 Recalibration Function Test  12-OCT-1984 9:10:20
Test # 21 Address Overflow Error Test  12-OCT-1984 9:10:21
Test # 22 Last Sector Transfer Test  12-OCT-1984 9:10:23
Test # 23 Test DMA Read With Invalid Map Registers  12-OCT-1984
9:10:24
Test # 24 Register Modification Refused Test  12-OCT-1984
9:10:27
Test # 25 Data Transfer Abort Test  12-OCT-1984 9:10:28
Test # 26 Read Header and Read Data Test  12-OCT-1984 9:10:31

SUMMARY REPORT:
    TOTAL # ERRORS = 0 (0 SYSTEM. 0 DEVICE. 0 HARD. 0 SOFT)
    12-OCT-1984 9:11:30
```